

**In the Claims:**

Please amend the claims as follows:

1. (Currently Amended) An insulated gate planar power device with high packing density of the elementary cells that compose it, comprising:

~~\_\_\_\_\_ having a~~ co-integrated Schottky diode electrically in parallel to the device formed in the area of each cell defined by an aperture through a polysilicon gate electrode, the polysilicon gate electrode being insulated from the underlying semiconductor by a dielectric gate layer, and being insulated from a source contact through a first dielectric layer formed on a top surface of the polysilicon gate and being insulated laterally from the source contact through a dielectric spacer, and wherein the first dielectric layer and dielectric spacer have thicknesses that are independent of diffusion conditions of a body region and a doping level of the polysilicon gate, and through which such a co-integrated cell structure is constituted, each elementary cell comprising:

~~\_\_\_\_\_ a the~~ body region formed in the semiconductor coupled to an invertible channel region under said insulated polysilicon gate electrode for establishing conditions of inversion of said channel region,

~~\_\_\_\_\_ a~~ source region formed in the area of said cell aperture within said body region,

~~\_\_\_\_\_ a~~ drain region in said semiconductor coupled to said invertible channel region,

~~\_\_\_\_\_ a~~ trench formed in said semiconductor in a portion of the area of said cell aperture having a depth extending from the surface of the semiconductor through said source region and said body region, a source metal layer contacting over the sides of said trench said source region and said body region for establishing a source contact and said drain region at the bottom of said trench to establish a Schottky diode contact, electrically in parallel to the elementary cell of the integrated insulated gate device, ~~characterized in that~~wherein

said trench is self aligned to the dielectric spacers formed on the definition edges surfaces of said aperture in a portion of the area of the aperture that includes a central "window" defined in a shade pattern of slanted body dopants implant, for a greater depth than the bottom of said source region and sufficient to expose at the bottom of the trench said drain region in the semiconductor bordered by

said body region at least along two opposite sides, and the depth of the trench being less than a depth of the body region;

said contact metal fills said central trench establishing an electric contact with said source region and with said body region on at least a portion of the surface of the lateral sides of said trench and said Schottky contact on at least a portion of the bottom surface of said trench.

2. (Withdrawn) The device of claim 1, characterized in that it further comprises a second deep body region, more heavily doped of said first body region, laterally contained in said first body region, but extending in said semiconductor for a greater depth than said first region, for shielding deeper the drain zone under said Schottky contact at least along two opposite sides.

3. (Withdrawn) The device of claim 1, characterized in that it further comprises, in said semiconductor, a buried region having the same type of conductivity of said first body region, formed under and at a depth from said Schottky contact established at the bottom of said trench.

4. (Currently Amended) The device according to claim 1, ~~characterized in that~~wherein said drain region in said semiconductor is an epitaxial layer grown on a semiconducting crystal with electrical characteristics different from that of said epitaxially grown layer.

5. (Currently Amended) The device according to claim 1, ~~characterized in that it~~wherein the device comprises an-is-a N channel device.

6. (Withdrawn) A process for fabricating an insulated gate integrated power device comprising the steps of:

- a) constituting a drain semi conducting substrate doped with a dopant of a first type of conductivity and forming an edge structure of the insulated gate integrated power device,
- b) forming an insulated gate electrode by growing or depositing a dielectric film of gate oxide on the surface of said drain semiconducting substrate and depositing thereon a conductive layer of polysilicon,

- c) covering said conductive polysilicon layer with an insulating layer or multilayer of dielectric material deposited thereon,
- d) depositing a layer of photo resist on said deposited insulating layer,
- e) defining said gate electrode by masking and anisotropic selective etching of said deposited insulating layer and of said polysilicon layer forming apertures through the area of which the integrated structure and the relative source contact of each elementary cell constituting said power device will be formed,

and characterized in that the successive sequence comprises the steps of

- f) performing a first ion implantation of a dopant appropriate to constitute a body region of opposite type of conductivity of said drain semiconducting substrate with certain tilt and twist angles such to determine a shade zone inside said aperture in function of the total height of the definition edge of the stack composed of said polysilicon layer, said insulating layer and said layer of photo resist, and of the width of the aperture, with an implant dose and energy appropriate to obtain a certain concentration and channel length;
- g) performing at least a second ion implantation at the same conditions of said first implantation but with different tilt and twist angles to define a central window in the shade pattern on the implanted cell area;
- h) removing of said layer of photo resist;
- i) activating the implanted dopants by heat treatment;
- j) performing a source ion implantation on the whole area of said aperture of a dopant of the same type of conductivity of the drain substrate and opposite to that of the dopant of said body implantations with dose and energy of implant appropriate to constitute a source region surrounded by said body region;
- k) activating of the implanted source dopant by heat treatment;
- l) depositing a sacrificial layer of a dielectric material under conditions of substantial uniformity of thickness of deposition over the steps of the definition borders of said apertures;

- m) anisotropic etching of the sacrificial layer for leaving a dielectric spacer on the definition edge surfaces of said apertures;
- n) anisotropic etching of the semiconductor for a depth deeper than the depth of said source region but shallower than the depth of said body region, exposing within the area of each cell surfaces of said source region, of said body region and, at the bottom of the trench, a zone of said drain substrate surrounded laterally by said body region;
- o) opening of contacts on said gate electrode through a dedicated photo resist mask;
- p) removing the photo resist mask and depositing one or more conductive metal layers for establishing inside said trench an electric contact with both the source region and the body region and determining a good barrier height of the Schottky contact established with the drain substrate on at least a portion of the bottom surface of said trench.

7. (Withdrawn) A process for fabricating an insulated gate integrated power device comprising the steps of:

- a) constituting a drain semi conducting substrate doped with a dopant of a first type of conductivity and forming an edge structure of the insulated gate integrated power device,
- b) forming an insulated gate electrode by growing or depositing a dielectric film of gate oxide on the surface of said drain semi conducting substrate and depositing thereon a conductive layer of polysilicon,
- c) covering said conductive polysilicon layer with an insulating layer or multilayer of dielectric material deposited thereon,
- d) depositing a layer of photo resist on said deposited insulating layer,
- e) defining said gate electrode by masking and anisotropic selective etching of said deposited insulating layer and of said polysilicon layer forming apertures through the area of which the integrated structure and the relative source contact of each elementary cell constituting said power device will be formed,

and characterized in that the successive sequence comprises the steps of

- f) performing a first ion implantation of a dopant appropriate to constitute a deep body region of opposite type of conductivity of said drain semi conducting substrate with certain tilt and twist angles such to determine a shade zone inside said aperture in function of the total height of the definition edge of the stack composed of said polysilicon layer, said insulating layer and said layer of photo resist, and of the width of the aperture, with an implant dose and energy appropriate to obtain a certain concentration and depth of implant;
- g) performing at least a second ion implantation at the same conditions of said first implantation but with different tilt and twist angles to define a central window in the shade pattern on the implanted cell area;
- h) removing said layer of photo resist;
- i) performing at least a third ion implantation of a dopant appropriate to constitute a body region of opposite type of conductivity of said drain semi conducting substrate with certain tilt and twist angles such to determine a shade zone inside said aperture in function of the total height of the definition edge of the stack composed of said polysilicon layer and said insulating layer, and of the width of the aperture, with an implant dose and energy appropriate to obtain a certain concentration and channel length;
- j) performing at least a fourth ion implantation at the same conditions of said third implantation but with different tilt and twist angles to define a central window in the shade pattern on the implanted cell area
- k) activating the implanted body and deep body dopants by heat treatment;
- l) performing a source ion implantation on the whole area of said aperture of a dopant of the same type of conductivity of the drain substrate and opposite to that of the dopants of said body and deep body implantations, with dose and energy of implant appropriate to constitute a source region surrounded by said body region;
- m) activating the implanted source dopant by heat treatment;

- n) depositing a sacrificial layer of a dielectric material under conditions of substantial uniformity of thickness of deposition over the steps of the definition borders of said apertures;
- o) anisotropic etching of the sacrificial layer for leaving a dielectric spacer on the definition edge surfaces of said apertures;
- p) anisotropic etching of the semiconductor for a depth deeper than the depth of said source region but shallower than the depth of said body region, exposing within the area of each cell surfaces of said source region, of said body region, and, at the bottom of the trench, said deep body region and a zone of said drain substrate surrounded laterally by said deep body region;
- q) opening of contacts on said gate electrode through a dedicated photo resist mask;
- r) removing the photo resist mask and depositing one or more conductive metal layers for establishing inside said trench an electric contact with both the source region and the body region and determining a good barrier height of the Schottky contact established with the drain substrate on at least a portion of the bottom surface of said trench.

8. (Withdrawn) A process of fabrication of a device according to claim 6, characterized in that it comprises the further step of carrying out, after having defined the gate electrode with the formation of said apertures, an ion implantation at sufficiently high energy for implanting a dopant of the same type of conductivity of the dopant used for realizing said body region in a buried region at a depth deeper than the bottom of said body regions, with a dose insufficient to compensate completely the dopant concentration of opposite type of conductivity of said drain substrate to create a shielding region under the Schottky contact.

9. (Withdrawn) An insulated gate planar power device with a Schottky diode in parallel thereto, said Schottky diode being realized by contacting with a metal layer a semiconductor substrate of a first type of conductivity and the contact zone being laterally surrounded by one or more diffused regions of opposite type of conductivity formed in said substrate for shielding the electric field under conditions of reverse bias of the diode, characterized in that it comprises, in said semiconducting

substrate, a buried region doped with a dopant of opposite type of conductivity to that of said semiconductor substrate, geometrically located under said Schottky contact zone and at a greater depth than the depth of said diffused regions.

10. (Withdrawn) The device of claim 9, wherein said buried region has the same type of conductivity of the semiconducting substrate but has a reduced resultant doping level.

11. (Withdrawn) A process of fabrication of an insulated gate planar power device according to claim 9, comprising the steps of:

- a) constituting a drain semi conducting substrate of a first type of conductivity,
- b) forming an insulated gate electrode by growing or depositing a dielectric film of gate oxide on the surface of said drain semiconducting substrate and depositing a conductive polysilicon layer;
- c) covering said polysilicon layer with an insulating layer of dielectric material deposited thereon,
- d) depositing a layer of photo resist on said insulating layer,
- e) defining said gate electrode by masking and anisotropic selective etching of said deposited insulating layer and of said polysilicon layer forming apertures through the area of which discrete structures or elementary cell of integrated structures said power device will be formed,

and characterized in that the successive sequence comprises the steps of

- f) performing a first ion implantation of a dopant appropriate to constitute a body region of opposite type of conductivity of said drain semi conducting substrate with certain tilt and twist angles such to determine a shade zone inside said aperture in function of the total height of the definition edge of the stack composed of said polysilicon layer, said insulating layer and said layer of photo resist, and of the width of the aperture, with an implant dose and energy appropriate to obtain a certain concentration and channel length;
- g) performing at least a second ion implantation at the same conditions of said first

implantation but with different tilt and twist angles to define a central window in the shade pattern on the implanted cell area;

- h) performing at least a third ion implantation at sufficiently high energy for implanting a dopant of the same type of conductivity of the dopant used to realize said body regions in a buried region at a greater depth than that of the bottom of said body regions, of and in a dose insufficient to compensate completely the dopant concentration of opposite type of conductivity of said drain substrate;
- i) removing said mask of photo resist;
- j) activating the implanted dopants by heat treatment;
- k) forming a spacer along the definition edge surfaces of at least an aperture destined to the formation of said Schottky diode there through;
- l) anisotropic etching of the semiconductor for a depth deeper than the depth of said body regions, exposing surfaces of said body region and of said drain substrate in a zone surrounded laterally by said body regions;
- m) depositing one or more conductive metal layers for establishing an electric contact with said body region and a good barrier height of the Schottky contact established with said drain substrate on at least a portion of the bottom surface of said etching of the semiconductor.

12. (Currently Amended) An insulated gate power device, comprising:

a drain region having a first conductivity type and having a surface;

an aperture having a first depth extending beyond the surface of the drain region and having sidewalls defined by adjacent first and second gate stacks, the gate stacks each including a polysilicon gate layer that is ~~being~~ electrically isolated from the aperture through a respective dielectric spacer;

first and second body regions formed in the drain region with each having a second conductivity type, the first body region having a portion adjoining the first gate stack and a portion adjoining a portion of the aperture, and the second body region having a portion adjoining the second gate stack and a portion adjoining a portion of the aperture, and the first and second body regions each having approximately a second depth that is greater than the first depth of the aperture;

a contact opening formed by a portion of the drain region defined between the portions of the first and second body regions adjoining the aperture;

first and second source regions formed in the first and second body regions, respectively, each source region having the first conductivity type and having a portion exposed on the corresponding sidewall of the aperture; and

a metal region formed in the aperture to the first depth, the metal region contacting the body and source regions and the contact opening, and wherein the polysilicon layer in each gate stack is further insulated from the metal region through a first dielectric layer formed on a top surface of the polysilicon layer, and wherein the first dielectric layer and dielectric spacers have thicknesses that are independent of diffusion conditions of the body regions and doping profiles of the polysilicon gate layers.

13. (Withdrawn) The insulated gate power device of claim 12 wherein first conductivity type is N-type and the second conductivity type is P-type.

14. (Withdrawn) The insulated gate power device of claim 12 further comprising first and second deep body regions formed in the first and second body regions, respectively, each deep body region having the second conductivity type.

15. (Withdrawn) The insulated gate power device of claim 12 further comprising a drain engineering implant region formed in the drain region.

16. (Original) The insulated gate power device of claim 12 wherein each gate stack comprises:

an oxide layer formed on a surface of the drain region;

a polysilicon region formed on the oxide layer;

an insulating layer formed on the polysilicon layer; and

an insulating spacer formed on the oxide layer and between the polysilicon and insulating layers to isolate these layers from the corresponding sidewall of the aperture.

17. (Withdrawn) A method of forming an insulated gate power device including a drain region having a first conductivity type and having a surface, the method comprising:

forming first and second gate stacks on the surface of the drain region;

forming an aperture between the gate stacks, the aperture extending beyond the surface of the drain region and having sidewalls defined by the gate stacks, the aperture being electrically isolated from the gate stacks;

implanting a dopant having the second conductivity type at a first angle relative to the sidewalls of the aperture to form a first body region in the drain region;

implanting a dopant having the second conductivity type at a second angle relative to the sidewalls of the aperture to form a second body region in the drain region, the second body region being formed adjacent the first body region to form a contact opening between portions of the first and second body regions adjoining the aperture;

forming first and second source regions in the first and second body regions, respectively; and

forming a metal region in the aperture, the metal region contacting the body and source regions and the contact opening.

18. (Withdrawn) The method of claim 17 wherein the operations of implanting a dopant are each performed multiple times to form the first and second body regions.

19. (Withdrawn) The method of claim 17 wherein the implanted dopant has a conductivity type that increases the resistivity of the drain region.

20. (Currently Amended) An electronic system including an insulated gate power device, the insulated gate power device comprising:

a drain region having a first conductivity type and having a surface;

an aperture having a first depth extending beyond the surface of the drain region and having sidewalls defined by adjacent first and second gate stacks, the gate stacks each including a polysilicon gate layer that is being electrically isolated from the aperture through a respective dielectric spacer;

first and second body regions formed in the drain region with each having a second conductivity type, the first body region having a portion adjoining the first

gate stack and a portion adjoining a portion of the aperture, and the second body region having a portion adjoining the second gate stack and a portion adjoining a portion of the aperture, and the first and second body regions each having approximately a second depth that is greater than the first depth of the aperture;

a contact opening formed by a portion of the drain region defined between the portions of the first and second body regions adjoining the aperture;

first and second source regions formed in the first and second body regions, respectively, each source region having the first conductivity type and having a portion exposed on the corresponding sidewall of the aperture; and

a metal region formed in the aperture to the first depth, the metal region contacting the body and source regions and the contact opening, and wherein the polysilicon layer in each gate stack is further insulated from the metal region through a first dielectric layer formed on a top surface of the polysilicon layer, and wherein the first dielectric layer and dielectric spacers have thicknesses that are independent of diffusion conditions of the body regions and doping profiles of the polysilicon gate layers.

21. (Original) The electronic system of claim 20 wherein the electronic system comprises a system that rectifies signals.

22. (Original) The electronic system of claim 20 wherein the rectifying system comprises a DC-DC converter.